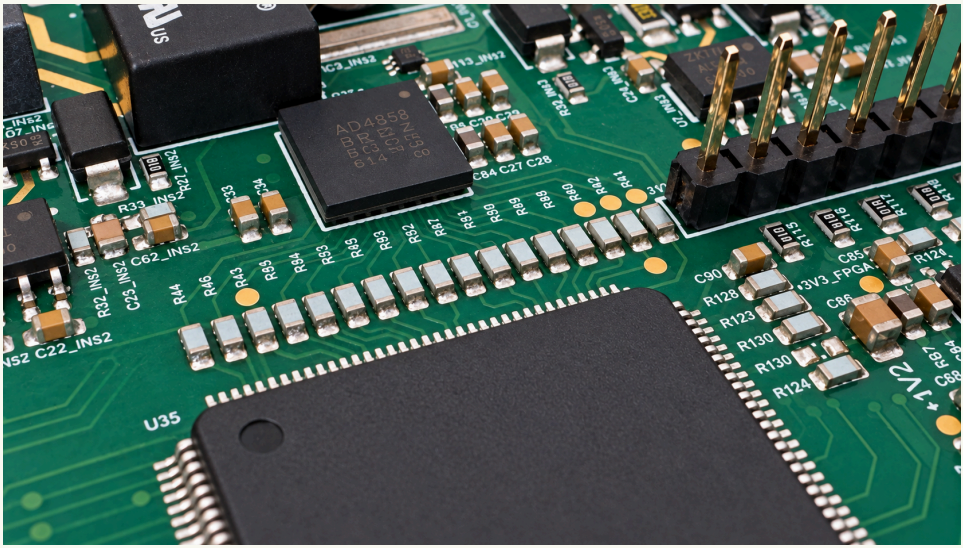
SMT / EMS

DFM Checklist

Design for manufacturability

Zoltan Erdei / ZANE systems



Your contract partner for electronics design and manufacturing.

01 / REVIEW RECORD

Project and review scope

Complete a separate record for each assembly revision and build variant.

Project / customer

Assembly part number / revision

Build variant / quantity

Reviewer / date

Contract / acceptance class / edition

Build site / process route

Review sequence

Gate A covers S01·S14. Complete it before releasing the design data for the first build. Gate B covers S15. Complete it using first-build records before releasing the next build.

Contents / 141 checks across 15 sections

S01	PCB Stackup & Material	2
S02	Design Rules & Clearances	2
S03	SMT Component Land Patterns	3
S04	Component Placement	4
S05	Solder Paste & Stencil	5
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GATE A / DESIGN RELEASE

Design review

Status: V = verified, O = open, N/A = not applicable. Blank = unreviewed.

S01 PCB Stackup & Material

☐	01.01	Layer sequence, finished thickness and copper weights agreed with the manufacturer in writing before layout is frozen.	CRIT
☐	01.02	Controlled-impedance nets identified: target values, tolerance, reference layers and test coupon position confirmed with the fabricator.	CRIT
☐	01.03	Laminate Tg and decomposition temperature checked against the actual reflow profile for the build — not a generic ≥ 150 °C figure.	CRIT
☐	01.04	CTE mismatch between laminate and large ceramic or metal-core components assessed; underfill or mounting strategy decided.	WRN
☐	01.05	Via construction (through, blind, buried, micro) agreed with the fabricator; aspect ratios within their drill capability.	CRIT
☐	01.06	Board outline, cutouts, slots and internal radii toleranced and confirmed against the panel fixture and conveyor rail width used at the manufacturer.	CRIT
☐	01.07	Copper balance checked per layer; isolated planes or heavy fills on one side flagged for bow and twist risk.	WRN
☐	01.08	Surface finish (ENIG, HASL, OSP, etc.) matched to component mix, shelf-life requirement and test probe compatibility.	CRIT
☐	01.09	Solder mask type, colour and LPI process confirmed; mask-defined vs copper-defined lands explicitly stated on fabrication notes.	WRN
☐	01.10	Outer copper pour strategy reviewed — hatching does not prevent solder wicking; stencil aperture design is the correct control.	WRN
☐	01.11	Board thickness tolerance stated; check against connector insertion force, press-fit retention and ICT fixture depth.	WRN
☐	01.12	Edge plating, castellations or half-vias specified with the fabricator; drill and plating process confirmed for the feature.	INFO
☐	01.13	Halogen-free, moisture-resistant or other special laminate requirement stated on fabrication notes where customer or application demands it.	WRN
☐	01.14	IPC Class (1, 2 or 3) and acceptance edition stated on fabrication drawing and agreed with the fabricator as the production standard.	CRIT

S02 Design Rules & Clearances

☐	02.01	Minimum trace width and spacing verified against the fabricator's stackup-specific DRC rules — not generic IPC defaults.	CRIT

Evidence / issue references

GATE A / DESIGN RELEASE

Design review

Status: V = verified, O = open, N/A = not applicable. Blank = unreviewed.

S02 Design Rules & Clearances (continued)

☐	02.02	Drill-to-copper, drill-to-drill and hole-to-edge clearances checked against the fabricator's finished-hole tolerance for each drill class.	CRIT
☐	02.03	Annular ring design allowance and finished-board acceptance criterion documented separately for each via type and IPC class.	CRIT
☐	02.04	Creepage and clearance distances verified against the applicable product safety standard (IEC 60601, IEC 60950, IEC 62368, or relevant EN) for the actual voltage, pollution degree and installation category.	CRIT
☐	02.05	Via-in-pad use justified; filling, capping and planarisation process agreed with the fabricator before layout is approved.	WRN
☐	02.06	Solder mask slivers between adjacent pads checked: ≥ 0.1 mm remaining web confirmed with the fabricator for their LPI process.	WRN
☐	02.07	Differential-pair routing reviewed for skew, length matching and layer transitions; return-path continuity confirmed.	WRN
☐	02.08	Current density and temperature rise under full load calculated for power and ground conductors; widths and copper weights adjusted accordingly.	WRN
☐	02.09	High-voltage isolation gaps in copper, mask and silkscreen layers verified as consistent with each other and with the safety standard.	CRIT
☐	02.10	Test-point net assignments and keepout clearances to adjacent components checked against the test access plan.	INFO
☐	02.11	All DRC violations in the CAD tool resolved or explicitly accepted with a documented rationale before release.	CRIT

S03 SMT Component Land Patterns

☐	03.01	Each land pattern traced back to the manufacturer's recommended footprint or IPC-7351 library entry; package drawing revision recorded.	CRIT
☐	03.02	Imperial vs metric package size codes distinguished throughout BOM and footprint library — mix-ups between 0402 imperial (1.0 × 0.5 mm) and 0402 metric (0.4 × 0.2 mm) cause assembly failures.	CRIT
☐	03.03	Passive end-cap geometry checked for thermal symmetry; tombstoning risk flagged where land or thermal mass differs between pads.	WRN
☐	03.04	Solder mask aperture confirmed as mask-defined or copper-defined per design intent; mask web width agreed with fabricator for fine-pitch parts.	WRN

Evidence / issue references _____

GATE A / DESIGN RELEASE

Design review

Status: V = verified, O = open, N/A = not applicable. Blank = unreviewed.

S03 SMT Component Land Patterns (continued)

☐	03.05	QFN and DFN exposed-pad aperture pattern designed to package manufacturer guidance; voiding target and inspection method agreed with the manufacturer at design release.	WRN
☐	03.06	BGA land geometry (NSMD vs SMD) and via treatment (tented, filled, capped) confirmed with the manufacturer for their paste-print and reflow process.	WRN
☐	03.07	Stencil aperture area ratio ≥ 0.66 verified for every aperture as a starting point; narrow apertures also checked for width-to-foil-thickness ratio. Confirm achievable window with stencil supplier.	CRIT
☐	03.08	Courtyard extents include maximum body tolerances and placement accuracy; no courtyard overlaps at design release.	WRN
☐	03.09	Component height verified against placement head, inspection camera, rework tool and enclosure clearances.	WRN
☐	03.10	Non-standard or customer-supplied package dimensions independently measured and footprint independently verified before adding to library.	CRIT

S04 Component Placement

☐	04.01	Pin 1, polarity and mating direction of every polarised or keyed device verified in 3D view and assembly drawing before layout is frozen.	CRIT
☐	04.02	Bottom-side component rotation convention confirmed with the manufacturer; ambiguous orientations in the pick-and-place file resolved in writing.	CRIT
☐	04.03	Board and panel fiducial pattern agreed with the manufacturer: at least three global fiducials for reliable machine registration; local fiducials added for fine-pitch devices where required.	CRIT
☐	04.04	Fiducial clearance to solder mask, copper and board edge confirmed; no silkscreen or vias within the camera field of the fiducial pad.	WRN
☐	04.05	Component-to-component spacing meets the minimum for the placement head, nozzle and inspection access used at the manufacturer.	CRIT
☐	04.06	Tall parts, through-board connectors and heatsinks checked for clearance to adjacent SMD pads, stencil travel and reflow fixture.	WRN
☐	04.07	Double-sided assembly sequence agreed; underside components assessed for weight, adhesive retention and second-pass reflow exposure.	WRN

Evidence / issue references _____

GATE A / DESIGN RELEASE

Design review

Status: V = verified, O = open, N/A = not applicable. Blank = unreviewed.

S04 Component Placement (continued)

☐	04.08	Components near board edge checked for conveyor rail clearance; keep-out zone for panel support pins confirmed with the manufacturer.	WRN
☐	04.09	Pick-and-place centroid file format, units, rotation convention and bottom-side interpretation agreed with the manufacturer before first build.	CRIT
☐	04.10	DNP (Do Not Populate) components marked unambiguously on placement data and assembly drawing; no open pads adjacent to DNP lands that could trap flux.	WRN
☐	04.11	Consistent component orientation used where it simplifies visual inspection — departures from the preferred direction justified and documented.	INFO

S05 Solder Paste & Stencil

☐	05.01	Stencil foil thickness selected for the smallest area-ratio-constrained aperture on the board; paste-volume requirements for all other components checked against that thickness.	CRIT
☐	05.02	Aperture area ratio ≥ 0.66 verified for every aperture at the selected foil thickness; aperture width ≥ 1.5× foil thickness for elongated openings.	CRIT
☐	05.03	Area ratio is a conventional starting point — actual paste-release window confirmed with the stencil supplier for the alloy, flux system and stencil-coat combination.	WRN
☐	05.04	Step stencil specified and step geometry agreed with the manufacturer where conflicting paste volumes cannot be resolved with a single foil thickness.	WRN
☐	05.05	QFN and exposed-pad apertures segmented per package manufacturer guidance; segmentation pattern reviewed against voiding acceptance criterion.	WRN
☐	05.06	Solder alloy specified (SAC305 default; deviation requires written approval); flux activity level and residue type agreed with the cleaning or no-clean process.	CRIT
☐	05.07	Paste handling, storage temperature and pot-life limits documented; SPI plan confirmed for the paste print process.	WRN
☐	05.08	Print-verification plan (SPI or first-article optical check) agreed with the manufacturer before first build.	WRN
☐	05.09	Stencil under-wipe interval and cleaning cycle established with the manufacturer based on board pitch and aperture density.	INFO

Evidence / issue references _____

GATE A / DESIGN RELEASE

Design review

Status: V = verified, O = open, N/A = not applicable. Blank = unreviewed.

S06 Thermal Design for Reflow

☐	06.01	Most thermally sensitive component identified from datasheets; its rated peak temperature and number of reflow cycles is the limiting constraint for the profile.	CRIT
☐	06.02	Thermocouple profiling plan agreed: measurement points at the limiting component, at large thermal masses, and at a corner pad of the smallest device.	CRIT
☐	06.03	Measured reflow profile validated against both the paste supplier's process window (minimum and maximum) and the component thermal limit — not just one of the two.	CRIT
☐	06.04	Large copper planes, heatsinks and thermal vias reviewed for uneven heating; auxiliary board support and fixture strategy agreed with the manufacturer.	WRN
☐	06.05	Via-in-pad and thermal-via arrays checked for solder wicking from the land; filled and capped vias required where wicking would starve the joint.	WRN
☐	06.06	Bare-board bow and twist measured per IPC-TM-650 2.4.22 before assembly; hot-assembly warpage is a separate phenomenon and assessed during profiling.	WRN
☐	06.07	Moisture sensitivity level (MSL) for every device identified per J-STD-020; storage, floor-life tracking and baking plan documented before parts are issued to production.	CRIT
☐	06.08	Hidden-joint inspection method (X-ray for BGA and QFN) agreed at design release; acceptance criteria and sampling plan recorded.	WRN
☐	06.09	Second-side reflow exposure assessed for all components assembled in pass 1; cumulative thermal exposure within component and solder joint ratings.	WRN

S07 THT Assembly Method

☐	07.01	Confirm whether this assembly variant has THT operations; mark this section N/A if it is SMT-only.	CRIT
☐	07.02	Finished hole diameter provides 0.1–0.3 mm annular clearance around the lead (per IPC-2222); lead-to-hole fit verified against fabricator's finished hole tolerance.	CRIT

Evidence / issue references _____

GATE A / DESIGN RELEASE

Design review

Status: V = verified, O = open, N/A = not applicable. Blank = unreviewed.

S07 THT Assembly Method (continued)

☐	07.03	Manual soldering workmanship standard (IPC-A-610 Class 2 or 3) agreed with the manufacturer; operator access to each joint confirmed in 3D view.	CRIT
☐	07.04	Thermal relief spoke width and count on plane connections balanced against fillet quality and current capacity — heavy planes without relief cause cold joints.	WRN
☐	07.05	Lead protrusion target and trim length specified; mechanical interference with enclosure or adjacent components checked after trimming.	WRN
☐	07.06	Connector and transformer mounting verified against PCB stress during mating cycles; strain relief or board support specified where needed.	WRN
☐	07.07	If the manufacturer cannot provide wave or selective soldering in-house, agree on an external EMS process and verify pallet/nozzle clearances, flux and thermal limits with that provider before design release.	WRN
☐	07.08	Mixed SMT + THT assembly sequence (which side soldered first, reflow then hand, or hand first) agreed and locked before BOM is finalised.	CRIT

S08 Cleaning & Contamination

☐	08.01	Cleaning requirement decided: no-clean flux leaving residue in-situ, or post-solder aqueous/solvent cleaning — decision recorded and traceability maintained through the supply chain.	CRIT
☐	08.02	Cleanliness acceptance criterion defined as a product- and process-specific figure, not a generic 1.5 µg NaCl/cm² default; test method (SIR, ionic contamination, visual) and sampling plan agreed.	CRIT
☐	08.03	Low-standoff parts (< 0.1 mm clearance) assessed for drainage and drying access; solvent trapping under BGAs and shielding cans flagged for the manufacturer's process review.	WRN
☐	08.04	Wash-sensitive components (unsealed connectors, microphones, speakers, coin cells) identified; masking or selective cleaning strategy agreed before first build.	CRIT
☐	08.05	If conformal coating is specified: coating material, coverage map, keep-out zones and masking drawing released alongside the PCB assembly drawing.	CRIT

Evidence / issue references _____

GATE A / DESIGN RELEASE

Design review

Status: V = verified, O = open, N/A = not applicable. Blank = unreviewed.

S08 Cleaning & Contamination (continued)

☐	08.06	Coating thickness measurement locations and acceptance method agreed with the manufacturer; inspection access confirmed in 3D layout before coating process is fixed.	WRN
☐	08.07	Flux residue compatibility with conformal coating confirmed with the coating supplier; activation class and residue volume within coating adhesion specification.	WRN

S09 Inspection & Test Access

☐	09.01	Inspection and test strategy decided at design start: AOI, SPI, ICT, flying probe, functional, or a combination — not retrofitted after layout is complete.	CRIT
☐	09.02	AOI accessibility confirmed for all solder joints on both sides; shadowed joints behind tall components identified and alternative inspection method agreed.	WRN
☐	09.03	Confirm X-ray access for every BGA, QFN and hidden-joint device. Check board and panel geometry against the field of view of the X-ray system selected by the manufacturer.	WRN
☐	09.04	ICT fixture requirements (pad size, pitch, keepout, board support) agreed with the test provider before layout is frozen; access to 100% of nets is the target.	WRN
☐	09.05	Flying-probe access requirements agreed with the manufacturer: minimum pad size, probe pitch and clearance differ from ICT and must be confirmed separately.	WRN
☐	09.06	Functional test connector or test-point header positions agreed and reserved in layout; mating connector and test harness availability confirmed.	WRN
☐	09.07	In-circuit and functional test coverage documented; untested nets listed and risk accepted in writing by the customer.	INFO
☐	09.08	Test points not doubled as via pads unless via is filled and planarised; bare via barrels are not reliable probe targets.	WRN
☐	09.09	Programming interface (JTAG, SWD, UART, proprietary) accessible with board assembled in production configuration; pin header or pogo-pin target agreed.	WRN

Evidence / issue references _____

GATE A / DESIGN RELEASE

Design review

Status: V = verified, O = open, N/A = not applicable. Blank = unreviewed.

S09 Inspection & Test Access (continued)

☐	09.10	First-article inspection plan references IPC-A-610 acceptance class agreed for the contract; any deviations from the standard recorded in the waiver log.	CRIT

S10 Silk Screen & Documentation

☐	10.01	All designators, pin 1 indicators and polarity marks legible at 3× magnification with the component fitted; no text hidden under component bodies.	WRN
☐	10.02	Reference designators unique across the entire assembly (including sub-boards and daughter cards); no duplicates in BOM or placement file.	CRIT
☐	10.03	Assembly drawing shows each side independently with visible reference designators, orientation and polarity at 1:1 scale.	CRIT
☐	10.04	BOM cross-checked against schematic, placement data and assembly drawing by designator, quantity, variant and DNP status before release.	CRIT
☐	10.05	Pick-and-place centroid file exported from the CAD tool and verified against the BOM: same designators, same quantity, same orientation convention.	CRIT
☐	10.06	Gerber or ODB++ package verified by opening in a CAM viewer separate from the CAD tool; layer stack-up and drill file alignment confirmed.	CRIT
☐	10.07	Warning or caution symbols for high-voltage, ESD-sensitive or polarity-critical areas present on the silkscreen and in the assembly drawing.	WRN
☐	10.08	Revision, date and document number on every released drawing; version consistent across schematic, PCB, BOM and assembly drawing.	CRIT
☐	10.09	Customer part number, manufacturer reference and IPC acceptance class stated on fabrication notes and visible on the bare board (ident mark or data matrix).	INFO
☐	10.10	Any hand-assembly instruction (solder sequence, torque value, adhesive type) captured in a separate work instruction — not embedded in silkscreen alone.	WRN

Evidence / issue references _____

GATE A / DESIGN RELEASE

Design review

Status: V = verified, O = open, N/A = not applicable. Blank = unreviewed.

S11 Panelisation

☐	11.01	Panel design agreed with the manufacturer before fabrication order is placed: board array, rail dimensions, fiducials, tooling holes and scoring method confirmed.	CRIT
☐	11.02	Rail width, tab count and tab spacing confirmed as within the conveyor and fixture capabilities of both the fabricator and the manufacturer — no generic figures assumed.	CRIT
☐	11.03	V-score angle, depth and keep-out from copper confirmed with the fabricator; residual web thickness consistent across the panel.	WRN
☐	11.04	Router tab (breakaway) positions and stub lengths agreed with the manufacturer; tab location away from edge-sensitive connectors and brittle ceramic components.	WRN
☐	11.05	Depanelisation stress assessed for components within 5 mm of V-score or router lines; ceramic capacitors, crystal oscillators and fine-pitch BGAs are highest risk.	WRN
☐	11.06	Panel fiducials visible and unobstructed on both top and bottom; at least one fiducial on each rail for reliable conveyor registration.	CRIT
☐	11.07	Board orientation within the panel chosen to optimise paste-print direction and thermal gradient uniformity through the oven.	INFO
☐	11.08	Panel mass and dimensions within the handling limit of the manufacturer's pick-and-place line and reflow oven conveyor.	WRN
☐	11.09	Singulated board dimensions and edge quality after depanelisation verified against the enclosure or connector mating tolerance.	WRN

S12 Component Sourcing & BOM

☐	12.01	Every BOM line carries manufacturer name, full manufacturer part number and a confirmed approved alternative; no "to be advised" entries at design release.	CRIT
☐	12.02	Long-lead and allocation-risk parts identified; minimum stock level or buffer purchase agreed before production order is placed.	CRIT
☐	12.03	Electrolytic and tantalum capacitor polarity, vent clearance and mounting orientation confirmed against package manufacturer's specification — not assumed from a generic rule.	WRN

Evidence / issue references

GATE A / DESIGN RELEASE

Design review

Status: V = verified, O = open, N/A = not applicable. Blank = unreviewed.

S12 Component Sourcing & BOM (continued)

☐	12.04	Component date-code sensitivity (electrolytic ESR, battery shelf life, photosensitive devices) noted in BOM; FIFO lot control requirement agreed with the manufacturer.	WRN
☐	12.05	Magnetic component shielding, orientation and coupling distance to adjacent magnetics reviewed for interference; application certification scope (CE/FCC or other) stated per project requirement.	WRN
☐	12.06	Counterfeit-risk parts (passive semiconductors, memory, legacy ICs) sourced from authorised distributors only; traceability evidence required at goods receipt.	CRIT
☐	12.07	Customer-supplied components: labelling, ESD packaging, shelf-life certificate and minimum incoming-inspection requirement agreed in writing with the manufacturer.	WRN
☐	12.08	BOM includes RoHS status, MSL rating, operating temperature range and package code system (imperial or metric) for every active device.	CRIT
☐	12.09	End-of-life or NRND parts flagged; last-time-buy quantity and alternative part qualification plan agreed before design release.	WRN

S13 ESD & Handling

☐	13.01	ESD-sensitive devices identified in BOM (JEDEC JS-001 class or equivalent); handling and packaging requirements stated on assembly routing card.	CRIT
☐	13.02	ESD Protected Area (EPA) controls — wrist straps, ESD-safe workbenches, floor mats, ionisers — confirmed as in place at the manufacturer for the relevant assembly operations.	CRIT
☐	13.03	PCB assembly packaging for inter-operation transfer and shipment specified: shielding bag, humidity indicator card and desiccant for MSL > 1 devices.	CRIT
☐	13.04	Board handling points and no-touch zones (connector contacts, exposed test pads, RF shields) identified on the assembly drawing and communicated to operators.	WRN
☐	13.05	Rework and repair bench ESD controls verified; soldering iron tip leakage current within IPC-A-610 limits.	WRN

Evidence / issue references _____

GATE A / DESIGN RELEASE

Design review

Status: V = verified, O = open, N/A = not applicable. Blank = unreviewed.

S13 ESD & Handling (continued)

☐	13.06	ESD event susceptibility of the assembled board in its final enclosure assessed; system-level ESD protection (TVS, spark gaps) confirmed by design.	WRN
☐	13.07	ANSI/ESD S20.20 compliance of the production environment confirmed or documented deviation accepted; audit records available for customer inspection.	INFO

S14 Lead-Free & RoHS Compliance

☐	14.01	Assembly confirmed as lead-free (SAC305 or equivalent) unless a specific exemption under RoHS 2011/65/EU Annex III or IV is documented and in scope.	CRIT
☐	14.02	All ten restricted substances under RoHS 2011/65/EU (Pb, Hg, Cd, Cr^{6+}, PBB, PBDE, DEHP, BBP, DBP, DIBP) checked; supplier DoC obtained for every BOM line.	CRIT
☐	14.03	Component termination finish (SnAgCu, NiPdAu, matte Sn) compatible with the manufacturer's lead-free solder process; tin whisker risk on pure Sn finishes noted and mitigated by design or finish selection.	WRN
☐	14.04	PCB surface finish (ENIG, HASL LF, OSP) confirmed as lead-free; mixed surface finish on a single board flagged for solderability and process compatibility review.	WRN
☐	14.05	REACH SVHC content ≥ 0.1% w/w per article checked; supplier SVHC declaration obtained and retained for every substance on the current ECHA candidate list.	WRN
☐	14.06	Conflict-minerals reporting scope (Dodd-Frank or OECD Due Diligence Guidance) determined by customer or market requirement; CMRT collected from relevant suppliers.	INFO
☐	14.07	Any non-RoHS components used under exemption documented with the exemption number, expiry date and rationale; exemption status confirmed current at time of manufacture.	CRIT
☐	14.08	RoHS technical documentation retained per Article 7(1): technical file available for ten years from placing on the market; EU Declaration of Conformity drafted and signed.	CRIT

Evidence / issue references

GATE B / FIRST ARTICLE

First-build verification

Complete using first-build records before releasing the next build.

S15 First Article & Process Validation

☐	15.01	First-article inspection scope agreed with customer before build: dimensional verification, IPC-A-610 workmanship audit, electrical test, and any customer-specific FAI requirement.	CRIT
☐	15.02	Where AS9102 Part B first-article inspection is contractually required, all AS9102 records completed and signed off; otherwise document the agreed FAI scope explicitly.	CRIT
☐	15.03	Solder paste print verified by SPI on the first panel: paste volume, area and offset within the stencil supplier's accepted process window.	CRIT
☐	15.04	Measured reflow profile recorded for the production oven and fixture configuration; profile file archived with the build record.	CRIT
☐	15.05	All hidden joints (BGA, QFN, LGA) X-rayed on the first article; void percentage and joint formation assessed against the agreed acceptance criterion.	CRIT
☐	15.06	Electrical test coverage (ICT or flying probe) completed; any net with less than 100% coverage listed with risk rationale accepted by the customer.	CRIT
☐	15.07	Any rework carried out on the first article performed to IPC-7711/7721; rework records (operator, method, material, before/after photos) retained in the build file.	WRN
☐	15.08	Build record includes: BOM lot traceability, paste batch, stencil ID, oven profile, inspection results, test results and operator sign-off — all retained for the agreed retention period.	CRIT
☐	15.09	Process deviation or non-conformance found at first article dispositioned (accept, rework, scrap or engineering change); corrective action closed before volume production is authorised.	CRIT

First article / lot ID

Test report / profile reference

Inspection record

Approved change / deviation reference

Applicable reference documents

Record the edition agreed for the project. IPC-7352 provides land-pattern guidance, IPC-7525 covers stencil design, J-STD-001 covers soldered assembly requirements, and IPC-A-610 covers assembly acceptability. Use the component drawing and contract requirements for the specific assembly.

RELEASE RECORD / DISPOSITION

Review and sign-off

Complete one decision per gate. Attach additional issue-log sheets as needed.

How to complete each row

Review every row in the current gate. V means verified with evidence; O means open and requires an issue-log entry. For N/A, give a reason in the log; a whole section may share one rationale. Blank means unreviewed. CRIT identifies a release blocker, WRN an issue that may be accepted by an authorised approver, and INFO an advisory observation.

Decision rules

HOLD	Any CRIT is open, any required review is incomplete, or a warning remains open without an approved waiver.
CONDITIONAL	All applicable critical checks are verified. Each open warning has a signed waiver, owner, condition and due date.
PASS	Every applicable critical and warning item is verified. Justified N/A rows are excluded. INFO observations alone do not block release.

Gate A / Release for first build

Decision: ☐ PASS ☐ CONDITIONAL ☐ HOLD

Approver / signature _____ **Date / issue-log reference** _____

Gate B / Release for next build

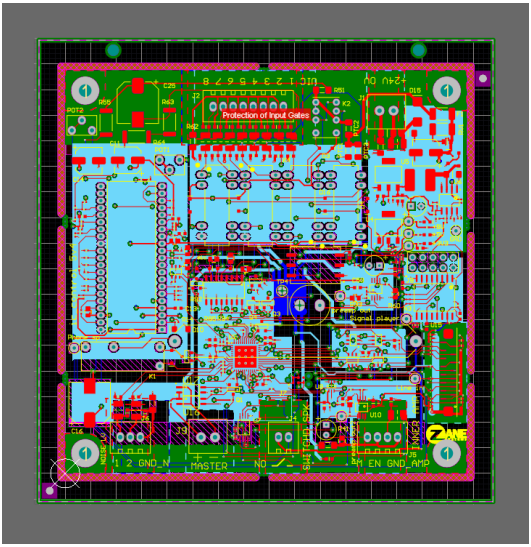
Decision: ☐ PASS ☐ CONDITIONAL ☐ HOLD

Approver / signature _____ **Date / issue-log reference** _____

ENGINEERING / COMPANY PROFILE

About ZANE systems

High-mix, low-volume PCB assembly in Hungary



We work with hardware teams whose products come in several variants and are built in small batches. Typical builds range from 2 to 1,000 boards. The same engineering and production team supports your first prototypes and repeat orders.

From design review to the first build

Our engineers review the layout, component choices and test access before assembly. We assemble and test boards in-house, including designs with 0201 components, fine-pitch ICs and micro-BGAs. Findings from the first build feed directly into the next revision.

Let’s review your next build

Have a board approaching release, or a family of assemblies you order in small batches? Send us your assembly files, BOM and quantities per variant. We can review the design together and quote the build.

sales@zane.hu / www.zane.hu